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10/604,962

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Allen et al.

Serial No.: 10/604,962

Group Art Unit: 2822

Filed: 08/28/03

Examiner: Siek, Vuthe

For: THE USE OF A LAYOUT-OPTIMIZATION TOOL TO INCREASE THE
YIELD AND RELIABILITY OF VLSI DESIGNS

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action mailed March 8, 2005, please amend the above-identified patent application as follows:

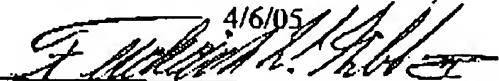
IN THE ABSTRACT

Please replace the Abstract as follows:

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Frederick W. Gibb, III